Notice of References Cited	Application/Control No. 10/064,157	Applicant(s)/Patent Under Reexamination GILDRED, JOHN	
	Examiner Shelton Austin	Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,275,239	08-2001	Ezer et al.	345/473
*	B	US-6,331,852	12-2001	Gould et al.	345/419
*	C	US-6,552,750	04-2003	Suen et al.	348/561
*	D	US-6,919,929	07-2005	Iacobelli et al.	348/589
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Smith, Douglas J., VHDL & Verilog Compared & Contrasted, Tutorial 48.1, 1996
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.